CLAIMS

What is claimed is:

1. A carry/majority circuit, comprising:

a plurality of differential transistor pairs coupled in parallel with each pair coupled on a first output end of said differential transistor pairs forming a respective leg and a second output end of said differential transistor pairs forming a pair of output nodes, wherein said differential transistor pairs have a single parallel gated level;

a pair of resistors coupled in parallel with a first end coupled to said differential transistor pairs at said respective output nodes; and

wherein current is steered through said leg of said differential transistor pairs having a higher input voltage.

2. The carry circuit according to claim 1, wherein a second end of said resistors are coupled to a ground and each said leg is coupled to a negative voltage supply.

3. The carry circuit according to claim 1, wherein a second end of said resistors are coupled to a positive voltage supply and each said leg is coupled to a ground.

4. The carry circuit according to claim 1, wherein each transistor of said differential transistor pairs is selected from the group consisting of: bipolar transistors, field effect transistors, metal oxide semiconductor field effect transistors, and insulated gate bipolar transistors.

5. The carry circuit according to claim 1, wherein said pair of resistors are matched.

6. The carry circuit according to claim 1, wherein a full differential between said output nodes occurs when all inputs or no inputs of said differential transistor pairs are a logic high.

7. The carry circuit according to claim 1, further comprising a buffer circuit coupled to said output nodes to provide a full differential between said output nodes regardless of inputs to said differential transistor pairs.

8. The carry circuit according to claim 7, wherein said buffer circuit is coupled to a clock.

9. The carry circuit according to claim 1, wherein a voltage level of said output nodes is calculated as the sum of said current multiplied by a resistance value of said resistor.

10. An accumulator architecture, comprising:
a carry section wherein said carry section operates as a single-level parallel-gated logic;
a latch section coupled to said carry section; and
at least one clock coupled to latch section.

11. The accumulator according to claim 10, wherein said carry section comprises a plurality of differential transistor pairs coupled in parallel.

12. The accumulator according to claim 10, wherein said carry section comprises a plurality of single ended input transistors coupled in parallel.

13. The accumulator according to claim 10, wherein said accumulator architecture is two gated levels.

14. The accumulator according to claim 10, further comprising a buffer circuit coupled to said pair of output nodes.

15. The accumulator according to claim 10, wherein said accumulator operates at a rate of at least 30GHz.

16. The accumulator according to claim 10, wherein said accumulator is fabricated by an indium phosphide (InP) heterojunction bipolar transistor (HBT) process.

17. A direct digital synthesizer, comprising:

a digital signal processor which generates a set of instructions;

an adder-accumulator that processes stored waveform data with said instructions and generates phase data, wherein said adder-accumulator includes a carry circuit having a single level parallel gated design with an integrated latch circuit;

a clock coupled to said adder-accumulator and said digital signal processor;

A phase to amplitude converter that processes said phase data that produces digitized waveform; and

a digital to analog converter that takes said digitized waveform and produces an analog synthesized output.

18. The synthesizer according to claim 17, further comprising a filter coupled to said digital to analog converter and an amplifier coupled to said filter.

19. The synthesizer according to claim 17, wherein said adder-accumulator further comprises a sum circuit with three series gated levels.

20. The synthesizer according to claim 17, wherein said carry circuit comprises a plurality of differential transistor pairs.